IN THE SPECIFICATION

Please replace the paragraph beginning on page 11, line 1 with the following replacement paragraph:

For example, assume with respect to register 200 that control word 110 is received as word 1. The bits within word 0 would then be assigned to be all logical zeroes to complete the values within register 200. However, diagonal XOR calculation chains 210 continue through word 0 as described previously. Consider diagonal XOR calculation chain 210a. Because only one set of XOR calculation chains will be used, XOR calculation chain 210a need not be complicated with the possible extraction points 220a, 220b, and 220c discussed with respect to prior art applications. Instead, XOR calculation chain 210a would have just a single extraction point 220d. ~~Having a single extraction point, the~~

Please replace the paragraph beginning on page 12, line 1 with the following replacement paragraph:

The resulting DIP calculation technique may be summarized with respect to Figure 3. At step 300, n words are demultiplexed from the native SPI4-2 bus. For example, with respect to register 200, words 3 through 0 are received. Then, at step 305, the n words are examined to see if control word 110 has been received. If control word 110 has not been received, the diagonal XOR calculation chains may be propagated through the n words in a conventional fashion and the result stored such as in inter-slice summing register 205 at step 310. If, however, the control word 110 was received, then words received after control word 110 in the set of n words are set to all logical zeroes at step 315. The diagonal XOR chains may then be propagated through the resulting n words to produce a value for 16-bit parity word 120 at step 320. At step 325 ~~320~~, 16-bit parity word 120 is shifted to the left one bit for

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each word that was set to all logical zeroes in step 315. After this adjustment, 16-bit parity word 120 may be collapsed into DIP4 parity word 135 in step 330.

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